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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/118,080	07/17/1998	WARREN M. FARNWORTH	M4065.067/P0	8629

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EXAMINER	
CHAMBLISS, ALONZO	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/118,080	FARNWORTH, WARREN M.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/29/02(request for reconsideration)* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-18 and 31-33* is/are pending in the application.

4a) Of the above claim(s) *19-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-18 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *18* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The request for reconsideration filed on 4/29/02 has been fully considered and made of record as Paper No. 17. Claims 1-7, 10-18, and 31-33 remain in the application, claims 8 and 9 have been canceled, and claims 19-30 are withdrawn from consideration.

Response to Arguments

2. Applicant's arguments with respect to claims 1-7, 9-18, and 31-33 have been considered but are moot in view of the new ground(s) of rejection.

However, the combination of Heo et al. and the Admitted Prior Art (Master Bond Polymer System EP31) discloses applicant's claimed invention. Heo discloses a semiconductor chip 11, a single dielectric layer 20 (i.e. multi-layer film having a non-conductive film layer 21), an electrically conductive lead 26 (i.e. conductive circuit pattern) on the dielectric layer 20, and adhesive 30 (i.e. epoxy) located between the semiconductor chip 11 and the dielectric layer 21 (see col. 5 lines 18-36; Fig. 4B). The information in the Master Bond Polymer System EP 31 technical data sheet is considered prior since this reference was cited in a PTO-1449 filed on 8/19/98 and is also as stated on page 8 lines 1-15 of the instant application, the known polymer is marketed as Master Bond Polymer System EP31 by Master Bond Inc., of Hackensack, New Jersey. The technical data sheet discloses an EP31 that is a two-component room temperature (i.e. room temperature) curing epoxy that cures at 75^0 F at 90% maximum strength developed within 24-36 hours and 150^0 F at 90% maximum strength developed

within 2-3 hours. Heo and the Admitted Prior Art both disclose substantially the same environment of an epoxy as an adhesive in structural bonding applications. Therefore, one skilled in the art would have readily recognized substituting the EP31 epoxy for the epoxy taught by Heo, since the EP31 epoxy has a high peel strength and good adhesion to a variety of materials including metals, plastics, rubbers, ceramics, and glass in structural bonding applications as taught by the Admitted Prior Art (Master Bond Polymer System EP31).

Claim Objections

3. Claim 13 is objected to because of the following informalities: the term " manufacturing " is improperly used in the preamble, since the term manufacturing is not given any patentable weight. It is suggested applicant delete the word " manufacturing." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 13 recites the limitation " said semiconductor chip " in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 4-7, 10-14, and 16-18, insofar as being definite, are rejected under 35 U.S.C. 103(a) as being unpatentable over Heo et al. (U.S. 5,858,815) in view of the Admitted Prior Art (Master Bond Polymer System EP31).

With respect to Claim 1, Heo discloses a semiconductor chip 11, a single dielectric layer 20 (i.e. multi-layer film having a non-conductive film layer 21), an electrically conductive lead 26 (i.e. conductive circuit pattern) on the dielectric layer 20, and adhesive 30 (i.e. epoxy) located between the semiconductor chip 11 and the dielectric layer 20 (see col. 5 lines 18-36; Fig. 4B). Heo fails to disclose a low temperature curing adhesive material that cures to about 90% of its maximum strength within 2 to 3 hours without exceeding 150^0 F. However, the Admitted Prior Art discloses an EP31 that is a two-component room temperature (i.e. low temperature) curing epoxy that cures at 90% maximum strength developed within 2-3 hours without exceeding 150^0 F. Heo and the Admitted Prior Art both disclose substantially the same environment of an epoxy as an adhesive in structural bonding applications. Therefore, one skilled in the art would have readily recognized substituting the EP31 epoxy for the epoxy taught by Heo, since the EP31 epoxy has a high peel strength and good adhesion to a variety of materials including metals, plastics, rubbers, ceramics, and

glass in structural bonding applications as taught by the Admitted Prior Art (Master Bond Polymer System EP31).

With respect to Claim 2, Heo discloses the dielectric layer 20 (i.e. multi-layer film) including polyimide, since the multi-layer film consist of non-conductive film 21 made of polyimide (see lines 4 col. 45-48 and col. 5 lines 10-17).

With respect to Claim 4, Heo discloses bond wires 40 connecting the semiconductor chip 11 to the electrically conductive leads 26 (see col. 5 lines 50-60;Figs. 2A, 4B, 5B).

With respect to Claim 5, Heo discloses a resin material 50 (i.e. epoxy which is a resin material) encapsulating the bond wires 40 (see col. 6 lines 55-63).

With respect to Claim 6, Heo discloses an opening 23 defined in the dielectric layer 20, wherein bond wires 40 and the resin material 50 are located in the opening (see col. 5 lines 18-24 and col. 6 lines 55-63; Figs. 6B, 7A, 7B, 7C, 8A).

With respect to Claim 7, Heo discloses a ball grid array 60 (i.e. a plurality of solder balls arranged in an array) on the leads 26 (see col. 5 line 30-36;Fig. 2B).

With respect to Claim 10, Heo discloses integrated circuits formed in a semiconductor material (i.e. semiconductor chip 11), a tape 21, 22 have openings 23 aligned with the integrated circuits that is connected to bond pads 12, wherein the tape 21, 22 includes a single layer 21 and electrically conductive leads 26 (i.e. conductive circuit patterns). The leads 26 are being printed (i.e. patterned) on the single dielectric layer 21. Bond wires 40 extend through the openings, wherein bond wires 40 are electrically connected to the integrated circuits (see col. 4 lines 35-67 and col. 5 lines

10-17; Fig. 2A, 2B, 4B, 5B). The adhesive material 30 is between the tape 21, 22 and the integrated circuits (see col. 5 lines 18-24;Figs. 2A, 4B, 5B). Heo fails to disclose an adhesive that cures to about 90% of its maximum strength within 24 to 36 hours at room temperature. However, the Admitted Prior Art discloses an EP31 that is a two-component room temperature curing epoxy that cures to about 90% of its maximum strength within 24 to 36 hours at room temperature. Heo and the Admitted Prior Art both disclose substantially the same environment of an epoxy as an adhesive in structural bonding applications. Therefore, one skilled in the art would have readily recognized substituting the EP31 epoxy for the epoxy taught by Heo, since the EP31 epoxy has a high peel strength and good adhesion to a variety of materials including metals, plastics, rubbers, ceramics, and glass in structural bonding applications as taught by the Admitted Prior Art (Master Bond Polymer System EP31).

With respect to Claim 11, Heo discloses a glob top encapsulant 50 (i.e. epoxy which forms a glob of material on top of bond wires 40) in the openings 23 (see col. 5 lines 55-62 and col. 6 lines 55-63; Figs. 6B, 7A, 7B, 7C, 8A).

With respect to Claim 12, Heo discloses a ball grid array 60 (i.e. a plurality of solder balls arranged in an array) for each of the integrated circuits, wherein the ball grid arrays are located on the electrically conductive leads 26 (see col. 5 line 30-36;Fig. 2B).

With respect to Claim 13, Heo discloses a single dielectric layer 20 (i.e. multi-layer film that includes a non-conductive film 21) having openings 23 with electrically conductive leads 26 (i.e. circuit patterns) associated with the openings 23, wherein the leads are being printed (i.e. patterned) on the dielectric layer 20 (see col. 4 lines 58-67

and col. 5 lines 45-67; Figs. 4B and 5B). The curing adhesive material 30 is located between a semiconductor chip 11 and the dielectric layer 20. Heo fails to disclose a low temperature curing adhesive material that cures to about 90% of its maximum strength within 2 to 3 hours without exceeding 150^0 F. However, the Admitted Prior Art discloses an EP31 that is a two-component room temperature (i.e. low temperature) curing epoxy that cures at 90% maximum strength developed within 2-3 hours without exceeding 150^0 F. Heo and the Admitted Prior Art both disclose substantially the same environment of an epoxy as an adhesive in structural bonding applications. Therefore, one skilled in the art would have readily recognized substituting the EP31 epoxy for the epoxy taught by Heo, since the EP31 epoxy has a high peel strength and good adhesion to a variety of materials including metals, plastics, rubbers, ceramics, and glass in structural bonding applications as taught by the Admitted Prior Art (Master Bond Polymer System EP31).

With respect to Claim 14, Heo discloses the dielectric layer 20 (i.e. multi-layer film) includes polyimide, since the multi-layer film consist of non-conductive film made of polyimide (see lines 4 col. 45-48 and col. 5 lines 10-17).

With respect to Claim 16, Heo discloses the dielectric layer 20 (i.e. multi-layer film) includes a metal alloy (i.e. circuit pattern 26 made of a copper foil) and a non-conductive film 21 made of polyimide (see col. 5 lines 10-17).

With respect to Claim 17, Heo discloses openings 23 that are slot-shaped to expose aligned bond pad 12 (see col. Figs. 4A, 4B, 5A, 5B).

With respect to Claim 18, Heo discloses openings 23 in the dielectric layer 20 (see col. 5 lines 48-55;Figs. 4B, 5B). The punched through feature in the claim is inherent in the reference, since any perforation in the dielectric layer 21 is equivalent to drilling or punching.

9. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heo et al. (U.S. 5,858,815) and the Admitted Prior Art (Master Bond Polymer System EP31) as applied to claims 1 and 13 above, and further in view of Chang et al. (U.S. 5,559,055).

With respect to Claims 3 and 15, Heo discloses a dielectric layer 20 (i.e. multi-layer film) including a non-conductive film 21 made of polyimide (see col. 5 lines 18-22). Heo-Admitted Prior Art both fail disclose a dielectric layer (i.e. insulating film) including a benzocylobutene. However, Chang discloses a dielectric layer including a benzocylobutene having the same dielectric constant as polyimide. Also, benzocylobutene is selected from the same group of dielectric materials as polyimide (see col. 4 lines 55-67, col. 6 lines 66 and 67, and col. 7 lines 1-3). Thus, benzocylobutene and polyimide behave in the same way in substantially the same environment, since benzocylobutene and polyimide are both low K dielectric materials, which provide protection for metal circuit patterns in semiconductor devices. Therefore, one skilled in the art would have readily recognize that benzocylobutene and polyimide are interchangeable, since benzocylobutene and polyimide are both low K dielectric material that provide protection for metal circuit patterns in semiconductor devices.

10. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heo et al. (U.S. 5,858,815) in view of Akagawa (U.S. 6,121,688).

With respect to Claim 31, Heo discloses a semiconductor chip 11, a single dielectric layer 21(i.e. non-conductive film), an electrically conductive leads 26 (i.e. conductive circuit patterns) on the single dielectric layer 21, and adhesive material 30 (i.e. polyimide) located between the single dielectric layer 21 and the semiconductor chip 11 (see col. 5 lines 10-24;Figs. 2A, 4B, 5B). Heo fails to explicitly disclose an anisotropically conductive adhesive material. However, Akagawa discloses an anisotropically conductive adhesive material as an insulation film (i.e. non-conductive film) on a circuit pattern 62 (see col. 11 lines 45-57). Thus, the anisotropically conductive adhesive material and polyimide adhesive material behave in the same way in substantially the same environment, since anisotropically conductive adhesive and polyimide adhesive both function as an insulating material. The anisotropically conductive adhesive functions as an insulating material, which provides an additional source of electrical connection for the semiconductor device. Therefore, one skilled in the art would readily recognize that anisotropically conductive adhesive and polyimide are interchangeable, since anisotropically conductive adhesive and polyimide adhesive both function as an insulating material and the anisotropically conductive adhesive functions as an insulating material, which provides an additional source of electrical connection for the semiconductor device.

With respect to Claim 32, Heo discloses via holes 23 (i.e. openings) defined in the single dielectric layer 21 and metal 40 (i.e. metal bond wires that provide electrical

signals to the leads 26) located in the via holes 23, wherein the metal 40 is connected to the leads 26 (see col. 5 lines 10-36; Figs. 4B, 5B).

With respect to Claim 33, Heo discloses a ball grid array 60 (i.e. a plurality of solder balls arranged in an array) on the leads 26, wherein the ball grid array 60 is located within the periphery of the chip 11 (see col. 5 line 30-36;Figs. 2B, 7B, 7C).

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

11. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

Alonzo Chambliss
Examiner
Art Unit 2827

AC/July 9, 2002